What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising:

a memory array comprising at least a first storage area and a second storage area, each of said at least first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array, said control circuit, responsive to a data transfer command, copies at least one sector from said first storage area to at least one sector in said second storage area without transferring the contents of said at least one sector to an external bus.

2. The memory device of claim 1, wherein said first and second storage areas are blocks.

3. The memory device of claim 1, wherein said at least one sector is a plurality of sectors.

4. The memory device of claim 3, wherein said plurality of sectors are adjacent sectors.

5. The memory device of claim 3, wherein said plurality of sectors include at least one sector not adjacent from at least one other sector.

6. The memory device of claim 1, wherein said memory is a non-volatile memory.

7. The memory device of claim 6, wherein said memory is a flash memory.

8. The memory device of claim 1, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

9. The memory device of claim 8, wherein said second block has at least as many sectors as said first block.

10. The memory device of claim 9, wherein said first and second blocks have identical number of sectors.

11. The memory device of claim 10, wherein each sector is a same size.

12. The memory device of claim 1, wherein said control circuit causes said at least one sector to be first copied from said first block to the buffer and subsequently copied from the buffer to said second block.

13. The memory device of claim 1, wherein said data transfer command includes a source address of a first sector in said first block and a destination address of a second sector in said second block.

14. The memory device of claim 13, wherein said data transfer command includes a length parameter specifying a total number of sectors starting from the source address which are copied to a corresponding number of sectors starting from the destination address.

15. The memory device of claim 13, wherein said data transfer command includes a count parameter specifying a number of additional sectors starting from the source address which are copied to a corresponding number of sectors starting at the destination address.

16. The memory device of claim 1, wherein said control circuit,

responsive to an erase command issued after the data transfer command, erases each sector of said first block; and

responsive to a second data transfer command issued after the erase command, copies the at least one sector from said second block to said first block.

17. The memory device of claim 1, wherein said control circuit further comprises:

a logic circuit for decoding commands; and

a state machine for executing decoded commands.

18. A memory system comprising:

a bus;

a controller coupled to said bus;

a memory coupled to said controller, wherein said memory further comprises:

a memory array comprising at least a first storage area and a second storage area, each of said at least first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array, said control circuit, responsive to a data transfer command, copies at least one sector from said first storage area to at least one sector in said second storage area without transferring the contents of said at least one sector to an external bus.

19. The memory system of claim 18, wherein said first and second storage areas are blocks.

20. The memory system of claim 18, wherein said at least one sector is a plurality of sectors.

21. The memory system of claim 20, wherein said plurality of sectors are adjacent sectors.

22. The memory system of claim 20, wherein said plurality of sectors include at least one sector not adjacent from at least one other sector.

23. The memory system of claim 18, wherein said memory is a non-volatile memory.

24. The memory system of claim 23, wherein said memory is a flash memory.

25. The memory system of claim 18, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

26. The memory system of claim 25, wherein said second block has at least as many sectors as said first block.

27. The memory system of claim 26, wherein said first and second blocks have identical number of sectors.

28. The memory system of claim 27, wherein each sector is a same size.

29. The memory system of claim 18, wherein said control circuit causes said at least one sector to be first copied from said first block to the buffer and subsequently copied from the buffer to said second block.

30. The memory system of claim 18, wherein said data transfer command includes a source address of a first sector in said first block and a destination address of a second sector in said second block.

31. The memory system of claim 30, wherein said data transfer command includes a length parameter specifying a total number of sectors starting from the source address which are copied to a corresponding number of sectors starting from the destination address.

32. The memory system of claim 30, wherein said data transfer command includes a count parameter specifying a number of additional sectors starting from the source address which are copied to a corresponding number of sectors starting at the destination address.

33. The memory system of claim 18, wherein said control circuit,

responsive to an erase command issued after the data transfer command, erases each sector of said first block; and

responsive to a second data transfer command issued after the erase command, copies the at least one sector from said second block to said first block.

34. The memory system of claim 18, wherein said control circuit further comprises:

a logic circuit for decoding commands; and

a state machine for decoded executing commands.

35. A method of transferring data in a memory device comprising at least a first and second blocks of storage locations, the method comprising:

(a) copying data from a first sector in the first block of said memory device to a buffer of said memory device;

(b) copying data from the buffer to a second sector in the second block of said memory device.

36. The method of claim 35, wherein said memory device is non-volatile.

37. The method of claim 36, wherein said memory device is a flash memory.

38. The method of claim 35, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

39. The method of claim 35, wherein said second block has at least as many sectors as said first block.

40. The method of claim 35, wherein said first and second blocks have identical number of sectors.

41. The method of claim 40, wherein each sector is a same size.

42. The method of claim 35, further comprising the steps of:

(c) receiving a count value from the external bus interface; and

(d) performing steps (a) and (b) repeatedly until a number of sectors adjacent to and after said first sector has been copied to corresponding sectors adjacent to and after said second sector;

wherein said number is equal to the count value.

43. The method of claim 35, further:

(c) receiving a length value from the external bus interface;

(d) performing steps (a) and (b) repeatedly until a number of sectors beginning with and adjacent to said first sector has been copied to a corresponding number of sectors beginning with and adjacent to said second sector;

wherein said number is equal to the length value.

44. The method of claim 35, further comprising:

(c) erasing said first block;

(d) copying data from the second sector to said buffer; and

(e) copying data from said buffer to said first sector.

45. A method for writing data into a non-volatile memory, comprising the steps of:

(a) responsive to receiving a data transfer command specifying a first address and a second address,

(1) copying data located at the first address of the memory to a buffer within the memory;

(2) copying data from the buffer to a second address of the memory;

(b) responsive to receiving an erase command specifying said first address, erasing at least a portion of said memory;

(c) responsive to receiving a data transfer command specifying said first address and said second address in reverse order,

(1) copying data located at said second address of the memory to the buffer;

(2) copying data from the buffer to the first address of the memory;

wherein each copy operation is performed without transferring data to an external bus of the memory.

46. The method of claim 45, wherein said memory is organized into a plurality of blocks and said first and second addresses are located in different blocks.

47. The method of claim 45, wherein said erase command erases the block which contains the first address.

48. A processor system comprising:

a processor;

a memory controller coupled to said processor;

a memory coupled to said controller, wherein said memory further comprises:

a memory array comprising at least a first storage area and a second storage area, each of said at least first and second blocks including a plurality of sectors;

a buffer;

a control circuit coupled to the memory array and the buffer for accepting external commands and for reading, writing, and erasing portions of said memory array, said control circuit, responsive to a data transfer command, copies at least one sector from said first storage area to at least one sector in said second storage area without transferring the contents of said at least one sector to an external bus.

49. The memory device of claim 48, wherein said first and second storage areas are blocks.

50. The memory device of claim 48, wherein said at least one sector is a plurality of sectors.

51. The memory device of claim 50 wherein said plurality of sectors are adjacent sectors.

52. The memory device of claim 50, wherein said plurality of sectors include at least one sector not adjacent from at least one other sector.

53. The memory device of claim 48, wherein said memory is a non-volatile memory.

54. The memory device of claim 53, wherein said memory is a flash memory.

55. The memory device of claim 48, wherein each sector of said second block has a size which is at least as large as each corresponding sector of said first block.

56. The memory device of claim 55, wherein said second block has at least as many sectors as said first block.

57. The memory device of claim 56, wherein said first and second blocks have identical number of sectors.

58. The memory device of claim 57, wherein each sector is a same size.

59. The memory device of claim 48, wherein said control circuit causes said at least one sector to be first copied from said first block to the buffer and subsequently copied from the buffer to said second block.

60. The memory device of claim 48, wherein said data transfer command includes a source address of a first sector in said first block and a destination address of a second sector in said second block.

61. The memory device of claim 60, wherein said data transfer command includes a length parameter specifying a total number of sectors starting from

the source address which are copied to a corresponding number of sectors starting from the destination address.

62. The memory device of claim 60, wherein said data transfer command includes a count parameter specifying a number of additional sectors starting from the source address which are copied to a corresponding number of sectors starting at the destination address.

63. The memory device of claim 48, wherein said control circuit,

responsive to an erase command issued after the data transfer command, erases each sector of said first block; and

responsive to a second data transfer command issued after the erase command, copies the at least one sector from said second block to said first block.

64. The memory device of claim 48, wherein said control circuit further comprises:

a logic circuit for decoding commands; and

a state machine for executing decoded commands.